An 8-GHz Continuous-Time Σ–Δ Analog-Digital Converter in an InP-based DHBT Technology

Sundararajan Krishnan[1], Dennis Scott[2], Miguel Urteaga[2], Zachary Griffith[2], Yun Wei[2], Mattias Dahlstrom[2], Navin Parthasarathy[2] and Mark Rodwell[2]

[1]Texas Instruments India Pvt. Ltd., Bangalore, 560017, India [2]University of California at Santa Barbara, Santa Barbara, CA 93106

Abstract **— An 8-GHz clock-rate second—order continuous-time Σ–Δ analog-digital converter achieves 57.4 dB, 51.7 dB and 40.2 dB SNR at signal sampling rates of 125 Ms/s, 250 Ms/s and 500 Ms/s, respectively. The ADC also achieves > 75 dBc of intermodulation suppression. The IC occupies a die area of 1.45mm^2, contains 76 transistors, and is fabricated in an InP-based HBT technology.**

I. Introduction

A popular oversampling ADC architecture is based on Σ–Δ modulation. These achieve high SNR without requiring high precision in component values or device matching. Moreover, the requirements on the analog anti-aliasing filter are significantly relaxed. Σ–Δ Modulators achieve high resolution by utilizing high sampling rates; a 2nd order ADC achieves a 15dB improvement in SNR for every octave increase in sampling rate.

InP-based heterojunction bipolar transistors have achieved very high device bandwidths [1], permitting very high-speed digital ICs. In bipolar processes, fast, low-offset switches are difficult to implement, and the continuous-time architecture is more readily implemented than the discrete-time switched-capacitor architecture prevalent in CMOS Σ–Δ ADCs. Continuous-time modulators have been reported with clock rates as high as 4 GHz [2] and 5 GHz [3]. Here, we report an 8-GHz clock-rate, second-order, continuous-time Σ–Δ ADC.

II. Fabrication

The circuit is fabricated in a triple-mesa process; both active-junctions are defined by selective wet-etch chemistry. Use of a controlled-impedance microstrip wiring environment with a Benzocyclobutene (BCB) transmission-line dielectric (5 μm thickness) and localized ground plane results in predictable parasitic capacitances and inductances for all IC interconnects, thereby improving the correlation between simulation and measured IC performance. RF measurements were done on a device with 0.7 X 8 μm^2 emitter mask and 1.7 X 12 μm^2 collector mask dimensions. The f_τ, f_{max} and the BV_{CEO} were found to be 205 GHz, 210 GHz and 6 V, respectively at a current density, $J_c = 2.5.10^5$ A/cm^2 and at a bias voltage, V_{ce} = 1.2 V.

III. Circuit Design

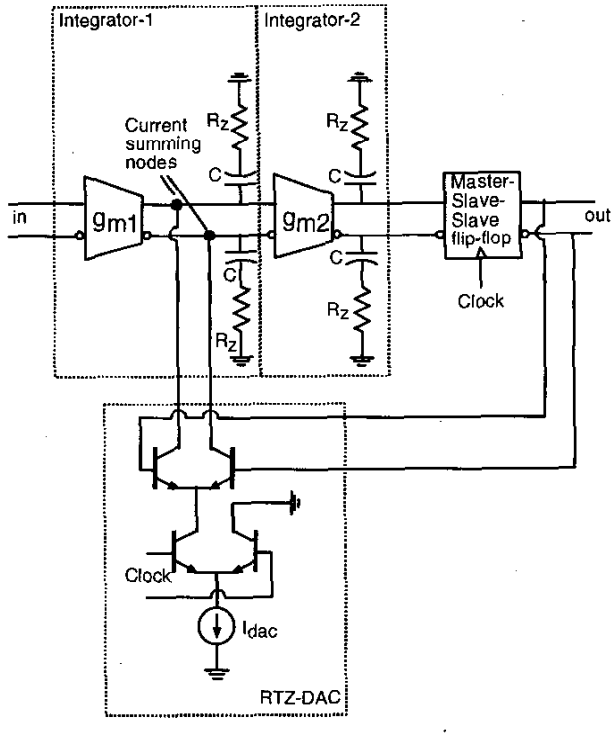

Figure 1: A simplified block diagram of the ADC

Fig. 1 shows a simplified block diagram of the IC. The ADC consists of two transconductance (g_m) cells, each followed by a passive integrator. The quantizer is an 87 GHz [4] master-slave-slave flip-flop and the DAC is a current-steering differential amplifier. The error signal is generated by current summing at the output nodes of the

0-7803-7695-1/03/$17.00 © 2003 IEEE

first transconductance cell. We achieve high linearity in the input transconductance cell by making its bias current much larger than the fed back DAC current. The quantizer uses an additional stage of regeneration to minimize metastability errors in the quantizer. This additional stage of regeneration introduces an excess delay of $T_{clk}/2$ in the loop. A return-to-zero (RTZ) DAC is used to reduce the excess delay to $T_{clk}/4$. The location of the zero in the loop is then altered suitably to neutralize the effect of the residual delay on the signal-to-noise ratio (SNR). The IC micrograph is shown in Fig. 2. The die area is 1.45 mm^2 and contains 76 transistors.

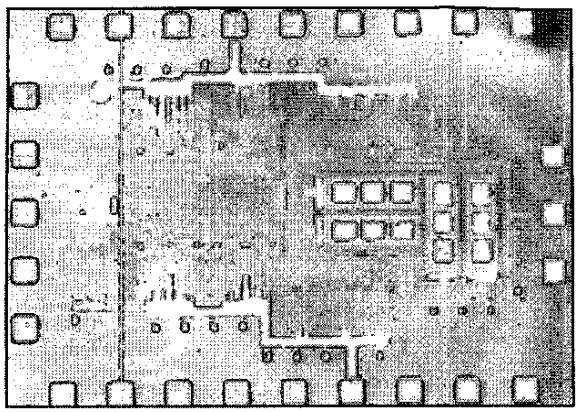

Figure 2: IC Micrograph of the ADC

IV. Measurement Technique and Results

For testing purposes, we directly capture the single-bit data stream of the Σ–Δ modulator and perform an FFT on the captured output to determine the performance of the ADC. Viewing the single-bit output on an analog spectrum analyzer performs the Fourier transform in real time and gives a qualitative indication of the ADC performance. However, the noise floor of the analog spectrum analyzer limits us to a dynamic range of 80 dB and hence, does not let us view the spectral-shaping of the noise at low frequencies. It is thus necessary to capture the digital data stream at the high data rates and perform the FFT to observe the spectral-shaping properties of the ADC. We capture the digital data stream by first demultiplexing it into 16 channels of 500 Msps each using a commercial 10G DEMUX. The data from the 16 channels is then read into a logic analyzer and transferred to a computer. The original 8 Gbps waveform is then reconstructed in software and a MATLAB-based program is used to perform a fast-Fourier transform (FFT) on this reconstructed waveform. We perform a 131072-point FFT for both one-tone and two-tone measurements.

Fig. 3 plots the calculated 131072-point FFT spectrum for a 62.5-MHz input. The oversampling ratio (OSR) is 64. We calculate the SNR and the effective number of bits of resolution (ENOB) by integrating the noise power over the signal bandwidth. The results are summarized in Table I. The ADC achieves SNR of 57.4 dB, 51.7 dB and 40.2 dB, corresponding to 9.25, 8.29 and 6.38 effective bits (ENOB) at signal sampling rates of 125 Msps, 250 Msps and 500 Msps, respectively, and dissipates 1.5 W of power. We do not observe any spectral-shaping of the noise for frequencies below 100 MHz. This is attributed to residual metastability errors in the quantizer and to delays associated with latch-latency.

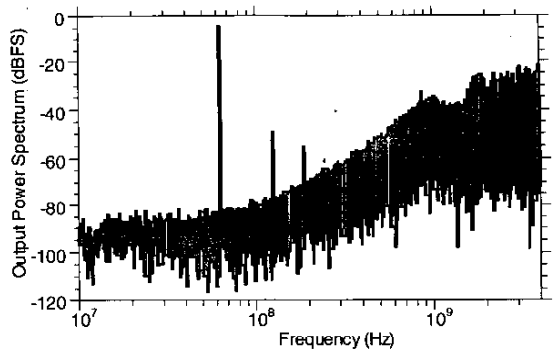

Figure 3: Output Power Spectrum of the ADC obtained by a 131072-point FFT on digital data acquired at 8 Gbps. The FFT bin size is 61 KHz.

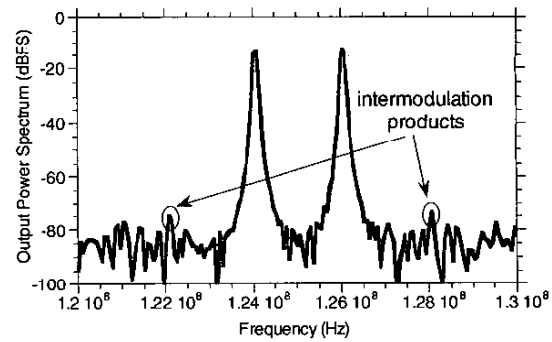

Figure 4: Output Power Spectrum of the ADC obtained by a 131072-point FFT on digital data acquired at 8 Gbps for a two-tone input; the two input tones are at 124 and 126 MHz.

We also performed two-tone measurements at 125 MHz to measure the linearity of the input transconductance cell. The two tones were spaced 2 MHz apart. An intermodulation suppression of 65 dBc is observed (Fig. 4). By changing the ratio of the integrator bias-current to the DAC bias-current, we were able to obtain > 75 dBc of

TABLE I

SNR AND ENOB as a function of frequency calculated by integrating the noise power over the signal bandwidth

Signal Frequency	Equivalent Sampling rate	SNR, dB (61 KHz)	SNR, dB (1 Hz)	SNR, dB (Nyquist)	ENOB
62.5 MHz	125 Msps	87.54	135.39	57.4	9.25
125 MHz	250 Msps	84.8	132.65	51.7	8.29
250 MHz	500 Msps	76.3	124.15	40.2	6.38

intermodulation suppression (Fig. 5). Based on these results, we can conclude that, at the cost of increased DC power, sufficient intermodulation suppression can be achieved by ensuring that the input stage overloads well after loop-overload occurs.

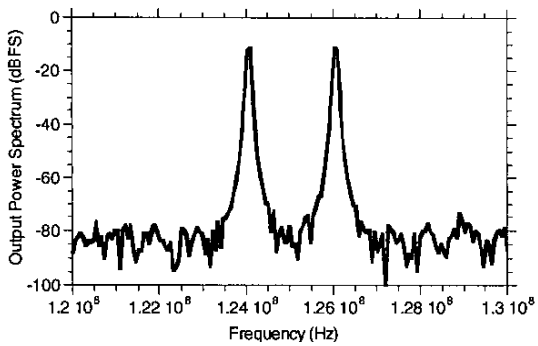

Figure 5: Output Power Spectrum of the ADC obtained by a 131072-point FFT on digital data acquired at 8 Gbps for a two-tone input; the two input tones are at 124 and 126 MHz; the bias point is varied to change the ratio of I_{bias}/I_{dac}

V. CONCLUSION

We have demonstrated an 8-GHz clock-rate, second-order, continuous-time Σ–Δ ADC. The ADC achieves SNR of 57.4 dB, 51.7 dB and 40.2 dB, corresponding to 9.25, 8.29 and 6.38 effective bits at signal sampling rates of 125 Msps, 250 Msps and 500 Msps, respectively. The IC occupies a die area of 1.45 mm^2, contains 76 transistors and dissipates 1.5 W of power.

ACKNOWLEDGEMENT

This work was supported by the Office of Naval Research (ONR) under ONR N00014-01-1-0024.

REFERENCES

[1] M. Dahlstrom, M. Urteaga, S. Krishnan, N. Parthasarathy, M. J. W. Rodwell, X. M. Fang, D. Lubyshev, Y. Wu, J. M. Fastenau and W. K. Liu, "Ultra-wideband DHBTs using a Graded Carbon-Doped InGaAs base," *post-deadline news, Indium Phosphide and Related Materials 2002*, Stockholm, Sweden, May 2002.

[2] G. Raghavan, J. F. Jensen, J. Laskowski, M. Kardos, M. G. Case, M. Sokolich and S. Thomas III, "Architecture, Design and Test of Continuous-Time Tunable Intermediate-Frequency Bandpass Delta-Sigma Modulators," *IEEE Journal of Solid State Circuits*, vol. 36, Issue 1, pp. 5-13, January 2001.

[3] A. Olmos, T. Miyashita, M. Nihei, E. Charry, Y. Watanabe, "A 5-GHz Continuous-Time Sigma-Delta Modulator Implemented in 0.4 μm InGaP/InGaAs HEMT Technology," *Proceedings of the 1998 IEEE International Symposium on Circuits and Systems*, pp. 575-8, 1998.

[4] S. Krishnan, Z. Griffith, M. Urteaga, Y. Wei, D. Scott, M. Dahlstrom, N. Parthsarathy and M. Rodwell, "87 GHz Static Frequency Dividers in an InP-based mesa DHBT Technology," *Technical Digest, 24th Annual GaAs IC Conference*, pp. 294-6, 2002.